X21 Controller

Description

The X21 communication controller is a microprocessor peripheral device. It supports the low level tasks regarding supervision of the X21 interface, protocol handling and data integrity checking being ensured by the microprocessor.

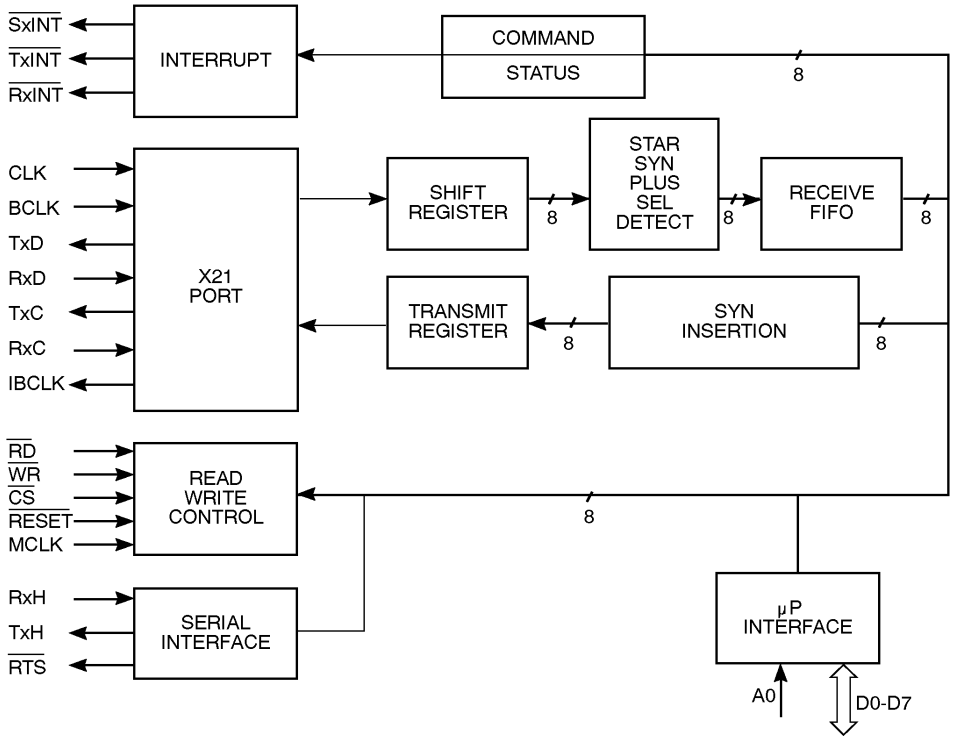
The circuit has an internal 8 bit architecture and allows direct memory access for high speed transfers. Data exchange can also occur through a fully transparent serial interface.

Application field includes video, voice or data transmission on circuit switched data networks and terminal adaptors (TA's) for ISDN (S interface -CCITT X30).

Features

- Compatible with CCITT X21 (1984/1988)
- 8 Bit data bus
- 3 interrupt sources
- Transparent serial interface
- Parity check, invalid state check
- Filtering of repetitive characters
- Receive FIFO (2 Characters)
- Internal or external byte clock
- Operation up to 2Mbits/s
- Low power CMOS

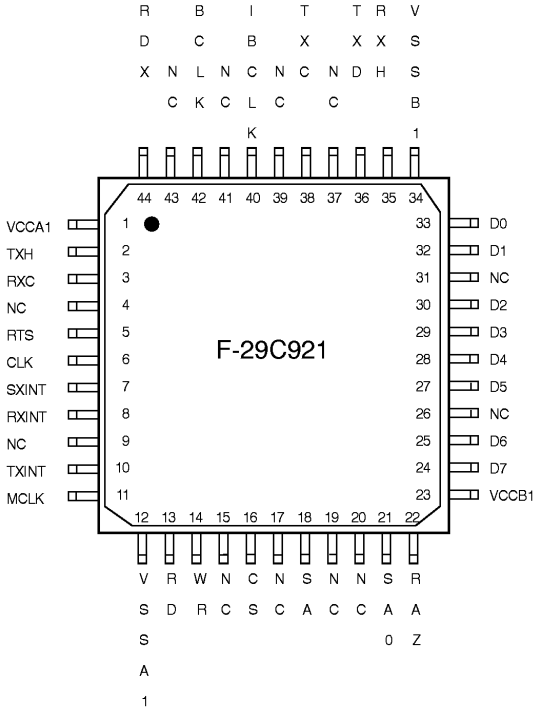
Figure 1. Block Diagram



Interface

Pin Configuration

Figure 2.



General Description

The MHS X21 controller is a microprocessor peripheral device which supports the CCITT X21 communication protocol (1984/1988).

This controller relieves the microprocessor from low level tasks associated with X21 call set-up and data transfers, thus reducing CPU software and component count.

Data can be sent to a 8 bit microprocessor or to synchronous serial data controllers including those conforming to HDLC. Data rate can reach 2Mbit/s. The 29C921 ensures call set-up and status change detection. Protocol handling and data integrity checking is done by the CPU.

X21 Protocol

The X21 protocol is based on handshaking with acknowledgement : when a terminal issues a status change to a slave station, the slave must respond before the terminal issues another status change. The 29C921 works equally on the data terminal equipment (DTE) side or on the data circuit terminating equipment (DCE) side.

As shown in *fig. 1*, the X21 physical interface consists of 2 data lines (T and R), 2 control lines (C and I), one data clock (S) and one optional byte clock (B). The byte clock can be generated by the 29C921.

Pin Description

Symbol	Pin Nº	Type	Name and Function
D7–D0	24, 25, 27, 28, 29, 30, 32, 33	I/O	Data bus : the data bus lines are bidirectional three state lines which interface with the system data bus.
A0	21	I	Data/register select (see table 1) – A0 = 0 the command or status register is addressed – A0 = 1 the transmit or receive register is addressed
SW	18	I	Must be held to 0
$\overline{RD}$	13	I	Read : read controls a data or status byte transfer from the CPU to the controller
$\overline{WR}$	14	I	Write : write controls a data or command byte transfer from the CPU to the controller
$\overline{CS}$	16	I	Chip select : this signal selects the controller and enables reading from or writing into its registers
MCLK	11	I	Master clock
TXD	36	O	Transmitter data (X21 port). Lead “T” seen from the DTE* side. Lead “R” seen from the DCE* side
TXC	38	O	Transmitter control (X21 port). Lead “C” seen from the DTE* side. Lead “I” seen from the DCE* side
RXD	44	I	Receiver data (X21 port). Lead “R” seen from the DTE* side. Lead “T” seen from the DCE* side
RXC	3	I	Receiver control (X21 port). Lead “I” seen from the DTE* side. Lead “C” seen from the DCE* side
CLK	6	I	Clock (X21 port) : lead “S” of the X21 interface
IBCLK	40	O	Internal byte clock : substitue for BCLK to synchronize the transmit data
BCLK	42	I	Byte clock (X21 port) : this clock is optional (lead “B”)
TXH	2	O	Transmitter data : this output transmits data on a serial interface
RXH	35	I	Receiver data : this input receives data from a serial interface
RTS	5	O	Request to send : this output signals that the circuit is ready to transmit data
RXINT	8	O (1)	Receiver interrupt : this output indicates that one character is present in the receive register (SR=1)
TXINT	10	O (1)	Transmitter interrupt : this output indicates that the transmit register is empty (SR=1)
SXINT	7	O (1)	Status interrupt : this output indicates a change in the status register contents
$\overline{RESET}$	22	I	Reset : used to reset all internal registers
V_{CC}A1/B1	1/23		Positive supply
V_{SS}A1/B1	12/34		Ground
NC	4, 9, 15, 17, 19, 20, 26, 31, 37, 39, 41, 43		Not connected

Notes : *DTE = Data Terminal Equipment.
*DCE = Data Circuit Terminating Equipment.
(1) Open drain.

Microprocessor Interface

The exchanges between the controller and the microprocessor system interface can be interrupt driven or direct memory access (DMA) driven.

The basic elements involved in these transfers are the following :

– 3 interrupt lines : $\overline{S \times INT}$, $\overline{T \times INT}$, $\overline{R \times INT}$.
– Command and status registers which can be directly addressed by the CPU.
– Transmit and receive data registers.

The access to the registers is monitored via input $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and A0.

When A0 = 0, the command ($\overline{WR}$ = 0) or status ($\overline{RD}$ = 0) register is addressed.

A0 = 1 enables the access to the transmit ($\overline{WR}$ = 0) or receive ($\overline{RD}$ = 0) data register.

A read operation to any register is enable by the $\overline{CS}$ pin ($\overline{CS}$ = 0) and The $\overline{RD}$ falling edge signal.

The internal read cycle is performed on the next MCLK rising edge signal.

A write operation to any register is enabled by the $\overline{CS}$ ($\overline{CS}$ = 0) and the $\overline{WR}$ rising edge signal.

The internal write cycle is performed on the next MCLK rising edge.

Figure 3. X21 Interface.

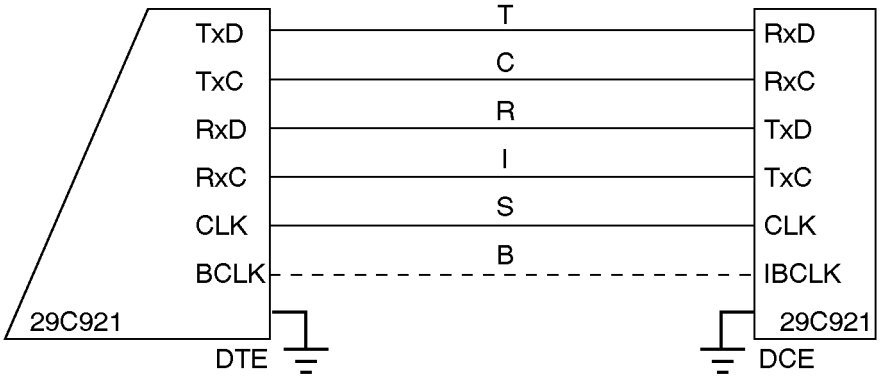


Table 1 : Register Select Decoding.

A0	$\overline{RD}$	$\overline{WR}$	Data	Addressed Register
0	1	0	D0/D7	COMMAND
	0	1		STATUS
1	1	0		TRANS DAT
	0	1		RECV DAT

Internal Registers

The circuit works under CPU control by means of 4 registers :

– Command register (CR).
– Status register (SR).
– Transmit data register (TR).
– Receive data register (RR).

Table 2 : Commande Register Set-up.

	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
0	µP INTERFACE	DISABLE $\overline{R \times INT}$	DISABLE $\overline{T \times INT}$	DISABLE $\overline{S \times INT}$	IBCLK	–	T × C = 0	–
1	SERIAL INTERFACE	ENABLE $\overline{R \times INT}$	ENABLE $\overline{T \times INT}$	ENABLE $\overline{S \times INT}$	BCLK	RESET	T × C = 1	LOOP MODE

* Command register

The command register is reset to 0 by the external $\overline{\text{RESET}}$ signal.

CR0 : Setting this bit to 1 produces a continuous transmission of the transmit register character.

CR1 : This bit directly drives the T × C control line.

CR2 : The circuit is reset when this bit is set to 1. CR2 must be held to 0 to allow the circuit to restart.

CR3 : When CR3 = 1, IBCLK output comes straight from BCLK input.
When CR3 = 0, IBCLK is internally generated using CLK input.

CR4 : Setting this bit to 1 enables a status change interrupt $\overline{S \times INT}$.

CR5 : Setting this bit to 1 enables a transmit interrupt $\overline{T \times INT}$.

CR6 : Setting this bit to 1 enables a receive interrupt $\overline{R \times INT}$.

CR7 : CR7 = 1 indicates that synchronous serial data transmission is achieved through the serial interface.
CR7 = 0 indicates that data are transferred through the µP interface.

Table 3 : Status Register set-up.

	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
0	–	–	–	–	–	RR EMPTY	–	R × C = 0
1	TR EMPTY	RR OVERLOAD	ERROR R × D	PARITY ERROR R × D	ERROR R × C	ONE CHARACTER RR	STATUS CHANGE	R × C = 1

* Status register

The status register is cleared by the external $\overline{\text{RESET}}$ line.

The bits of the status register are set independently of the state of the command register bits and in particular the interrupt bits (CR4 to CR6).

SR0 : This bit indicates the status of the R × C control line, after a stable state has been detected on this wire.

SR1 : This bit is set to 1 after detection of a status change on R × D or R × C.

SR2 : When the receive FIFO contains at least one character, this bit is set to 1. SR2 is cleared after the received character(s) has (have) been acquired.

SR3 : Set to 1 when an error is detected on the R × C input, namely when a non stable state lasts more than 24 “S” clock cycles.

SR4 : Set to 1 after a parity error detection on R × D, in synchronous mode (error = even parity).

SR5 : Set to 1 after an error detection on R × D input. This means that during more than 24 “S” clock cycles, the R × D wire is not in a stable state (00, FF, 55, 0F or 33) in asynchronous mode.

SR6 : This bit indicates an overload of the receive data register (RR) and that one character or more has been lost (SR6 = 1).

SR7 : When the transmit data register (TR) is empty, this bit is set to 1.

The error bits (SR3, SR4, SR5 or SR6), and bit SR1 are cleared whenever the status register is read.

* Transmit and receive data registers

The transmit register (TR) and receive (RR) can be read or written by the microprocessor or by a DMA. In that mode, interrupts $\overline{T \times INT}$ and $\overline{R \times INT}$ are used as DMA requests.

In microprocessor mode, the µP data transfers are controlled by $\overline{T \times INT}$ and $\overline{R \times INT}$. These interrupts are activated by the status bits SR7 and SR2. *(See paragraph “INTERRUPTIONS”).*

X21 Interface

* Receive operation

All status changes occuring on wires R × D and R × C are detected and processed by the 29C921.

- **Control Line**

When the circuit senses a stable state (”0” or “1”) during 16 clock periods on wire R × C, a status change interrupt ($\overline{S \times INT}$) is created, and bit SR0 from the status register stores the value of R × C.

If no stable state has been detected during 24 clock cycles, bit SR3 indicates an error and a status interrupt ($\overline{S \times INT}$)

is created. Reading the status register clear the error condition.

- **Data line**

– Asynchronous mode :

When the circuit senses a stable state (00, FF, 55, 0F or 33) during 16 periods on wire R × D, a status change interrupt ($\overline{S \times INT}$) is sent, and the detected value is written into the receive data register.

If no stable state has been detected during 24 clock cycles, bit SR5 shows an error and a $\overline{S \times INT}$ is created. This error is cleared when reading the status register.

– Synchronous mode :

The circuit will switch from asynchronous to synchronous mode after detection of two following "SYN" (16) characters. At the same time, a byte sync. clock is generated, and the received characters are compared with characters "PLUS", "BEL", "SYN" and " * ".

Going from asynchronous to synchronous mode does not generates as "$\overline{S \times INT}$" interruption.

Characters "SYN" are ignored. They are not loaded into the receive register (RR).

The first character "BEL", "PLUS" or " * " is transferred into register RR and generates a Receive Interrupt $\overline{R \times INT}$.

Following "BEL" "PLUS" or " * " characters are not loaded into the receive register (RR) but a status interrupt SXINT is sent for the second "BEL" "PLUS" or " * " character.

In synchronous mode, all characters different from " * ", "PLUS", "BEL" and "SYN" are loaded into the receive register and a receive interrupt $\overline{R \times INT}$ is sent.

When the circuit detects a stable state (00, FF, 55, 0F or 33) during 16 bit clock periods, it switches from synchronous to asynchronous mode and sends a status interrupt, SXINT. The parity error is not pointed out.

The first character corresponding to this stable state is always loaded into the receive register (RR) and generate a receive interrupt RXINT.

- **Parity check**

In asynchronous mode, the circuit conforms to X21 specification and checks that the received parity is odd.

Whenever a parity error is detected, bit SR4 (parity error) and SR1 are set in the status register. This will also generate a S × INT (depending on the state of bit CR4). However, the parity error is pointed out after reception of the character following the erroneous character.

Table 4 : Synchronous/Asynchronous Modes.

Mode	Symbol	Hexadecimal Mode
Asynchronous	0 1 10	00 FF 55 0F 33
Synchronous	SYN PLUS BEL * OTHER	16 AB 07 2A Code AI5

Switching from synchronous to asynchronous mode does not generate a parity error.

- **Transmit operation**

Control line

Bit CR1 from the command register directly controls the status of output T × C.

- **Data line**

Synchronous data including characters "SYN", " * ", "PLUS" and "BEL" are sent out from output T × D. The data are synchronous with BCLK, or with the internal byte clock IBCLK if BCLK is not used. The byte clock is selected through bit CR3.

Bits CR0 and CR7 both control the T × D output according to *table 5*.

Table 5 : Transmit Modes.

CR7 Serial Mode	CR0 Loop Mode	Transmit Operation
0	0	The circuit sends the character contained in the transmit register. If (TR) is empty, a $\overline{T \times INT}$ is generated, and a "SYN" character is sent.
0	1	The transmit register character is continuously sent to the line. A transmit interruption $\overline{T \times INT}$ is not generated.
1	X	The circuit sends the data received on input R × H from the serial port.

Serial Mode

Data can be exchanged through a µP bus, or through a synchronous serial data link in transparent mode. The µP mode is normally used for communication set-up and termination and the transparent mode for the data-transfer (state 5 of X21 spec.).

The serial mode is selected by setting CR7 = 1. This also drives output $\overline{RTS}$ to 0. The internal data paths are from input R × H to output T × D and from input R × D output T × H.

Note also that when CR7 = 0, output T × H = 1.

This mode allows an easy implementation of any communication protocol for data exchange through a synchronous transmitter/receiver (Transcom, Datex-L, Kilostream, DDS...).

The serial synchronous mode can also be implemented on the circuit termination side. In that case, input R × H and output T × H are linked to the data transmission network as shown in *figure 5*.

Figure 4. Serial Mode (terminal application using HDLC).

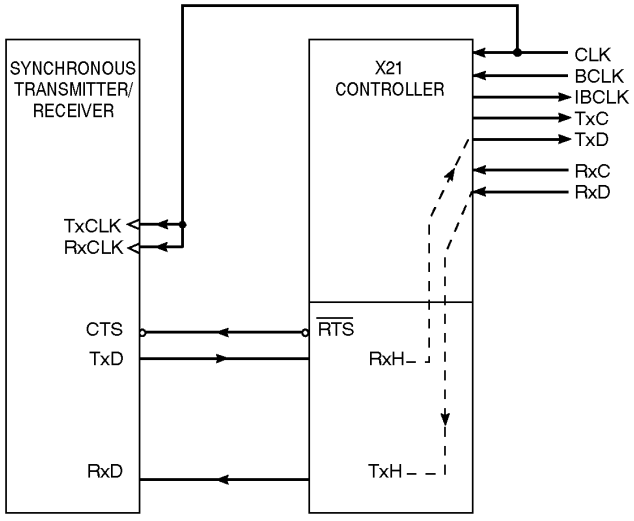
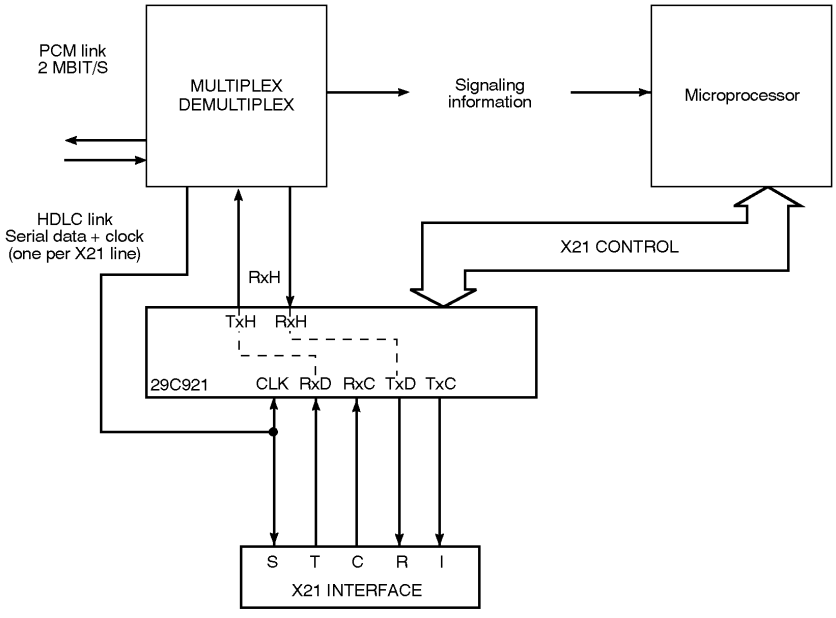


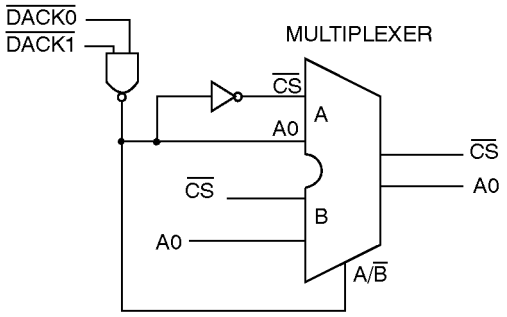
Figure 5. HDLC Mode (circuit termination application).



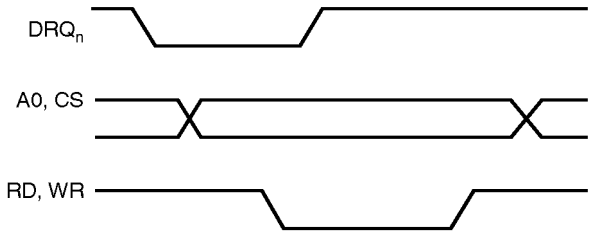
DMA Operation

Each 29C921 can be hardware configured to use up to 2 DMA channels : Transmit Channel and Receive Channel ; in this case $\overline{R \times INT}$ and $\overline{T \times INT}$ are used as DMA Request lines. Acknowledgement of a DMA cycle is done via normal data read or write cycles. This is accomplished by encoding the $\overline{DACK}$ signal to generate A0, $\overline{CS}$ and by multiplexing them with the normal A0, $\overline{CS}$ signals.

DMA Acknowledge Circuit



DMA Timing



Interruptions

- **Status interruption $\overline{S \times INT}$**

When enabled (CR4 = 1), this interruption is sent if :

SR1 = 1 → Status change on R × D or R × C.
SR3 = 1 → 1 Error detected on R × C.
SR4 = 1 → Parity error.
SR5 = 1 → Error detected on R × D.
SR6 = 1 → Overload in the receive register.

Reading the status register clears this interruption.

- **Receive interruption $\overline{R \times INT}$**

When enabled (CR6 = 1), this interruption will occur when a character has been received in register RR, or SR2 = 1.

Reading the receive registers clears this interruption.

- **Transmit interruption $\overline{T} \times$ INT**

When enabled (CR5 = 1), a transmit interruption is set when TR is empty, or SR7 = 1.

This interruption, and also bit SR7, cannot be set in loop mode (CR0 = 0).

Writing into the transmit register clears this interruption. All interruptions are cleared by an external reset ($\overline{RESET}$ = 0) or an internal reset (CR2 = 1).

Resetting a specific interruption through bits CR4, CR5 or CR6 in the command register will immediately cancel the corresponding interruption.

Electrical Characteristics

Absolute Maximum Ratings

V_{CC} to GND : . . . . . – 0.3 V to + 7 V
Input/output voltage : . . . . . – 0.3 V to V_{CC} + 0.3 V
Storage temperature : . . . . . – 65 ºC to 150 ºC

DC Electrical Characteristics

V_{CC} = 5 V ± 10 %, TA = 0°C to 70°C

Parameter	Min.	Max.	Unit	Conditions
Low level input voltage VIL		0.8	V	
High level output voltage VIH	2.2		V	
Low level output voltage VOL		0.4	V	IOL = 13.3 mA for D[7:0] IOL = 6.9 mA for TXD, TXC TXH, RTS, $\overline{RXINT}$, $\overline{TXINT}$, $\overline{SXINT}$, IBCLK.
High level output voltage VOH	2.4		V	IOH = – 13.3 mA for D[7:0] IOH = – 6.9 mA for TXD, TXC TXH, RTS, $\overline{RXINT}$, $\overline{TXINT}$, $\overline{SXINT}$, IBCLK.
Input leakage current IIL/IIH	– 4	+ 4	µA	Vin = 0 / Vin = Vccmax
3 state output leakage current IOZ	– 4	+ 4	µA	V_{CC} = 5.5 V
Standby current ICC0		50/80*	µA	Vin = V_{CC} or GND, outputs unloaded, clocks = V_{CC} or GND.
Operating current ICC1		10/18*	mA	V_{CC} = 5.5 V, MCLK = 7.5 MHz, VIL = GND, VIH = V_{CC}

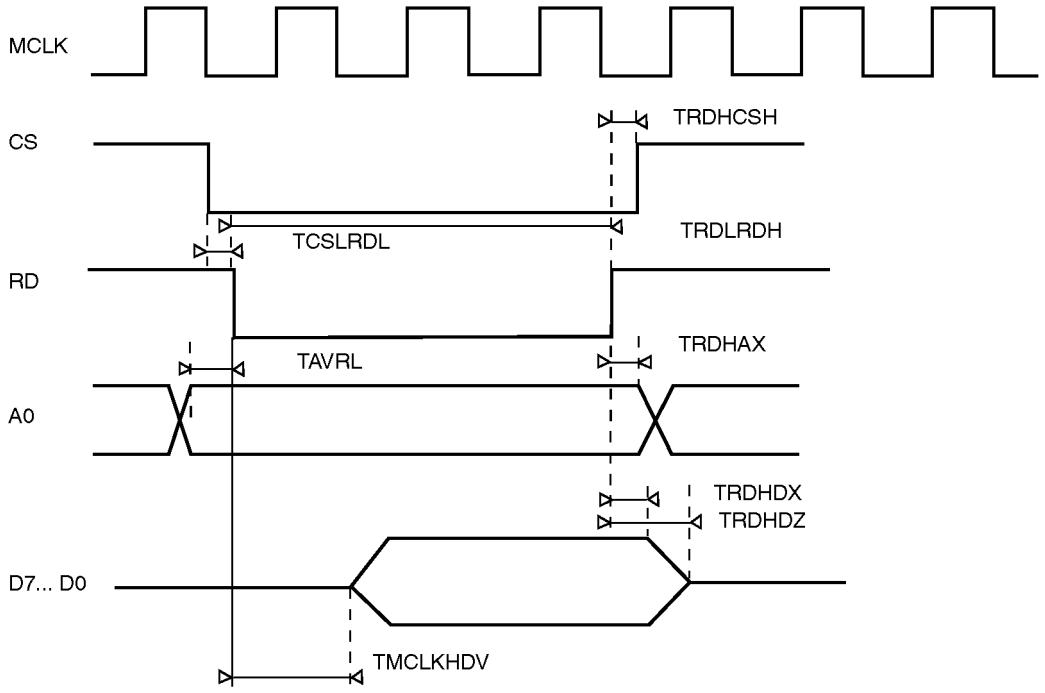
Outputs SXINT, RXINT, TXINT are open drain.
(*) TA = –40°C to 85°C

AC Characteristics

V_{CC} = 5 V ± 10 %, TA = – 40 °C to 85 °C

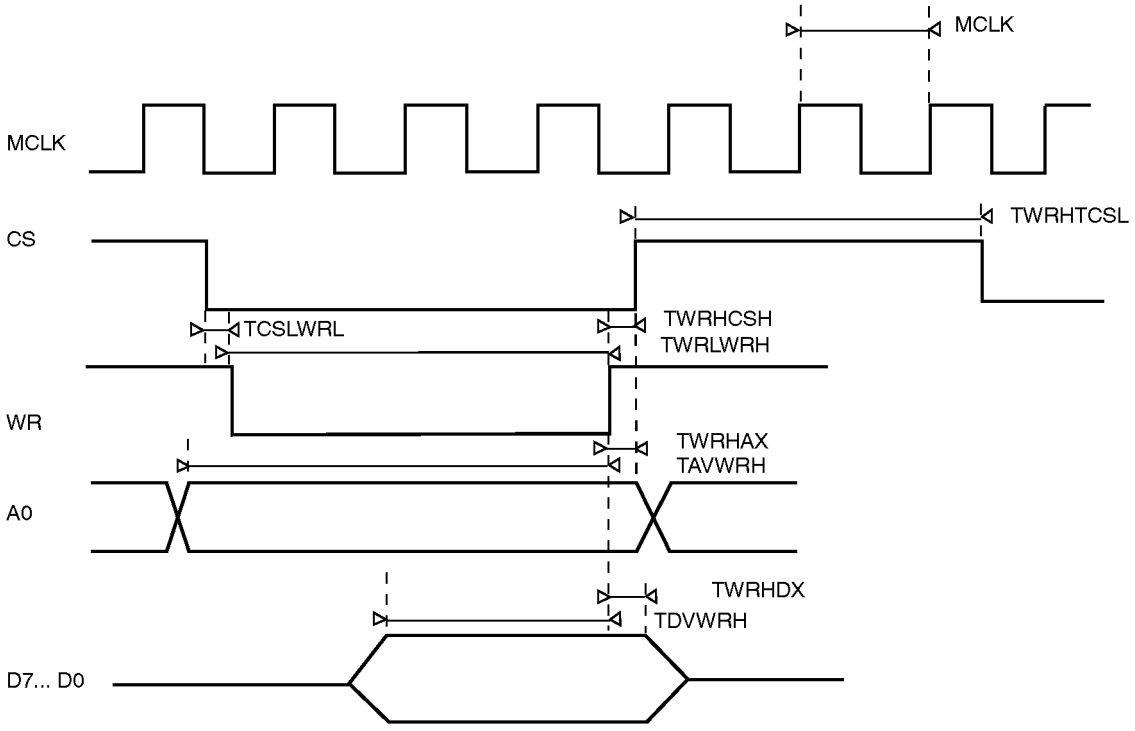
Load Circuit

Read Cycle



Symbol	Parameter	Typ	Min	Max	Unit
TAVRL	Address valid to read low set up time		0		ns
TRDLRDH	Minimum read pulse	100	MCLK + 35		ns
TCSLRDL	Chip select low to read low		0		ns
TMCLKHDV	MCLK high to data valid			30	ns
TRDHAX	Hold address from read high		0		ns
TRDHCSH	Chip select high to read high		0		ns
TRDHDX	Data hold from read high		7.5		ns
TRDHDZ	Data high Z from read high			MCLK + 30	ns

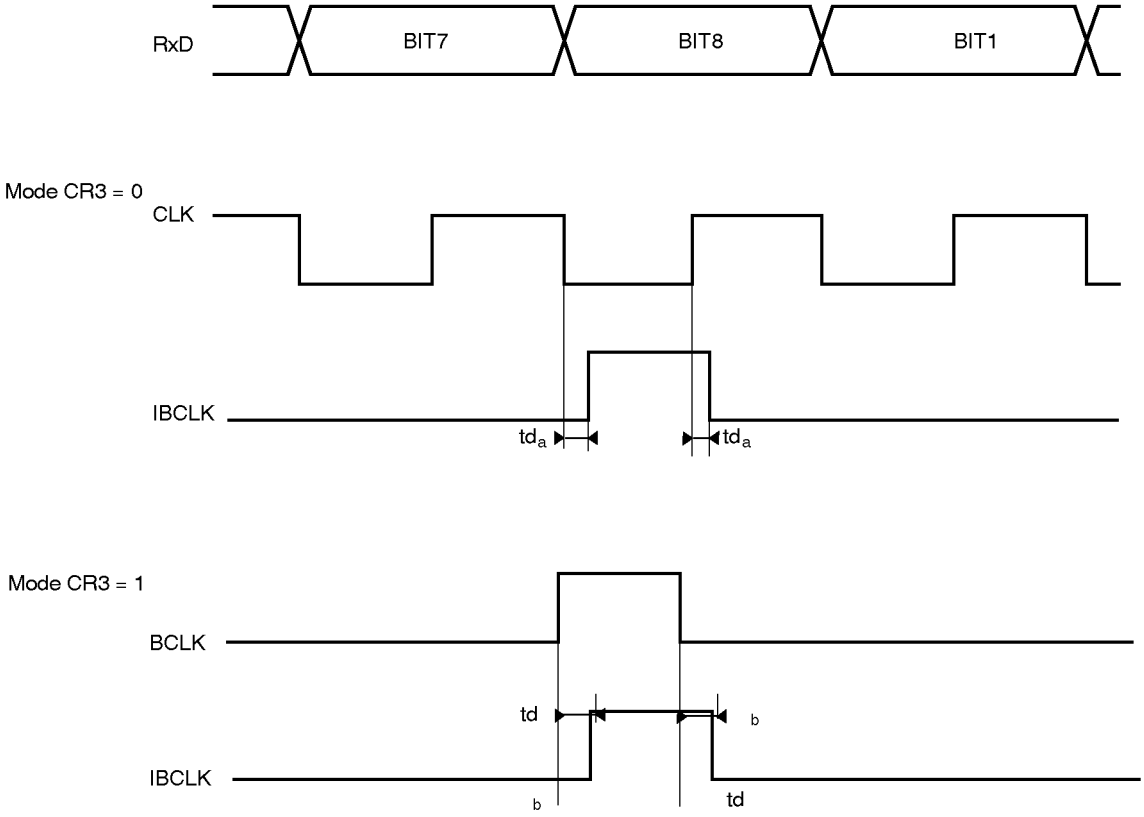
Write Cycle



Symbol	Parameter	Typ	Min	Max	Unit
TWRLWRH	Minimum write pulse	100	20		ns
TDVWRH	Data set up to write high	10	10		ns
TWRHDX	Hold data from write high	10	10		ns
TCSLWRL	Chip select low to write low		0		ns
TWRHAX	Hold address from write high	10	10		ns
TWRHCSH	Chip select high to write high		0		ns
TAVWRH	Address set up to write high	10	10		ns
TWRHTCSL	Write high to next access		2.5		MCLK

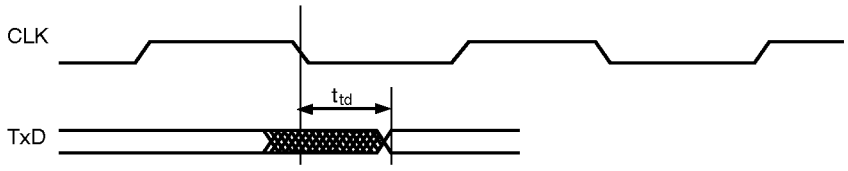
Clock Specification

FMCLK ≥ 2.5 FCLK



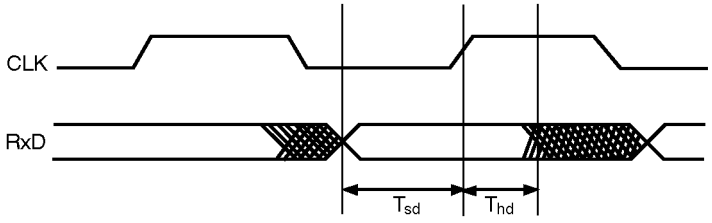
Symbol	Parameter	Min	Typ	Max	Units
tda	delay IBCLK/CLK	–	–	30	ns
tdb	delay IBCLK/BCLK	–	–	30	ns

Transmit Data Cycle



Symbol	Parameter	Min	Typ	Max	Units
t_{td}	delay TxD/CLK	–	–	30	ns

Receive Data Cycle



Symbol	Parameter	Min	Typ	Max	Units
t_{sd}	RXD valid to CLK high setup time	10	–	–	ns
t_{hd}	RXD hold time from CLK high	10	–	–	ns

Ordering Information